WHAT IS CLAIMED IS:

1. A clock synthesizing circuit for generating a plurality of lower frequency clock signals from a higher frequency clock for driving a pixel-based image sensor, said synthesizing circuit comprising:

a pixel rate generator that generates a master clock having a master clock frequency corresponding generally to a readout rate of the image sensor;

a frequency locked loop that receives the master clock and generates a high frequency clock operating at a multiple of the master clock frequency; and

a clock generation circuit that utilizes the high frequency clock to generate a plurality of low frequency clock signals for driving the image sensor.

2. The clock synthesizing circuit as claimed in claim 1 wherein the frequency locked loop is a phase locked loop.

3. The clock synthesizing circuit as claimed in claim 1 wherein the frequency locked loop is a delay locked loop.

4. The clock synthesizing circuit as claimed in claim 1 wherein the clock generation circuit utilizes the edge transitions of the high frequency clock to generate the plurality of low frequency clock signals for driving the image sensor.

5. The clock synthesizing circuit as claimed in claim 1 wherein the clock generation circuit generates a high frequency shift register clock for reading out the image sensor.

6. The clock synthesizing circuit as claimed in claim 1 wherein the clock generation circuit generates a high frequency reset clock for the image sensor.

7. The clock synthesizing circuit as claimed in claim 1 wherein the clock generation circuit includes a counter driven by the master clock that feeds one or more comparator pairs whose outputs are logically combined to form one or more pixel rate clocks with programmable rising and falling edge positions.

8. The clock synthesizing circuit as claimed in claim 1 wherein the clock generation circuit further generates one or more further low frequency clock signals for driving electronics associated with the image sensor.

9. The clock synthesizing circuit as claimed in claim 8 wherein the clock generation circuit generates high frequency clamp and sample clocks for a correlated double sampling circuit.

10. The clock synthesizing circuit as claimed in claim 8 wherein the clock generation circuit generates a high frequency clock for an analog to digital converter circuit.